DATA PROCESSING DEVICE AND DATA PROCESSING SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a Continuation Application of U.S. patent application Ser. No. 13/818,379, filed on Feb. 22, 2013, which is based on International Application PCT/JP2010/065054, filed on Sep. 2, 2010, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present invention relates to a data processing device and a data processing system, and particularly to a data processing device having a central processing unit and to a data processing system in which the data processing device is used.

BACKGROUND ART

[0003] Recently, with miniaturization of the data processing device including a central processing unit (CPU) configured on a semiconductor substrate, problems of a decrease of the breakdown voltage of transistors and an increase of the off-state leakage current have arisen.

[0004] Meanwhile, apparatuses using the data processing device are required to operate with an operating voltage, which is supplied to the data processing device, in a wide voltage range from a relatively high voltage (on the order of 5 V) to a relatively low voltage (3 V) and to a still lower voltage (1.8 V) in consideration of reduction of the power consumption, because of external factors (such as communication standards).

[0005] In order to operate in a wide voltage range, the data processing device has a plurality of power supply circuits (regulators) in the data processing device to generate an internal operating voltage from an externally supplied voltage and supply the generated voltage to internal functional blocks (see PTL 1), and determines the operation state of the power supply circuits in accordance with a signal based on the operation mode of the central processing unit (see PTL 2).

[0006] Also, in order to reduce the power consumption, the data processing device uses, as its internal voltage, a voltage generated by lowering an externally supplied voltage, and performs an intermittent operation in which a transition to a low power consumption state is made while operation is unnecessary. In the low power consumption state, the clock and the power supply voltage that are supplied to internal functional blocks of the data processing device are controlled. Specifically, the frequency of the clock to be supplied is lowered, the power supply voltage to be supplied is decreased, or supply of the clock and/or the power supply voltage is stopped (see PTL 3 and PTL 4).

CITATION LIST

Patent Literature

[0007] PTL 1: Japanese Patent Laying-Open No. 2002-83872

[0008] PTL 2: Japanese Patent Laying-Open No. 2001-211640

[0009] PTL 3: Japanese Patent Laying-Open No. 7-28549

[0010] PTL 4: Japanese Patent Laying-Open No. 2010-118746

SUMMARY OF INVENTION

Technical Problem

[0011] In the case where such a step-down power supply circuit is incorporated to generate an internal operating voltage, the self power consumption, namely the power consumed by the step-down power supply circuit itself hinders reduction of the power consumption.

[0012] For example, in a step-down power supply circuit shown in FIG. **2** of PTL 1, a driver MOS transistor **40** which lowers an externally supplied voltage to an internal operating voltage is designed, in order to reduce the self power consumption in the operation state in which the power consumption is maximum, so that the ON resistance in this operation state is minimum.

[0013] Also, in order to ensure adequate driving ability even when the externally supplied voltage is a low voltage, the width of the gate electrode of the MOS transistor **40** is increased and, in order to apply a higher voltage than an internal operating voltage to the gate electrode of the output MOS transistor **40**, the gate insulating film is thickened. Accordingly, the capacity of the gate electrode of the driver MOS transistor **40** is increased. In the case where the intermittent operation is performed and a transition is made from a low power consumption state to a normal operation state, it is a problem that increase of the voltage level of the internal operating voltage to be supplied to internal functional blocks is delayed. On the contrary, in the case where a transition is made from the normal operation state to the low power consumption state, it is a problem that draw of the charge having been supplied to the internal functional blocks, to the ground potential, is delayed, resulting in an unexpected increase of the internal supply voltage.

[0014] An object of the present invention is therefore to provide a data processing device and a data processing system that are capable of quickly raising the voltage level of an internal operating voltage to be supplied to internal functional blocks (load circuit) when the intermittent operation is performed.

Solution to Problem

[0015] A data processing device according to an embodiment of the present invention includes: a load circuit including a central processing unit and operated by supplied electric power; and a step-down power supply circuit stepping down an external power supply voltage and having an output node connected to the load circuit. The step-down power supply circuit includes: a first step-down unit stepping down the external power supply voltage; and a bias current control circuit controlling a magnitude of bias current flowing through an auxiliary path from the output node to a ground. The data processing device further includes a control unit increasing the magnitude of the bias current, prior to a change of an operation state of the load circuit by which a relatively large change occurs to an amount of current consumed by the load circuit.

ADVANTAGEOUS EFFECTS OF INVENTION

[0016] In accordance with an embodiment of the present invention, the voltage level of an internal operating voltage